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Case Study of 32nm, 22nm, 14nm and 10nm Semiconductor Process Technologies

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Abstract: Moore's law or Moore's prediction is an observation that, the number of transistors in a dense integrated circuit doubles approximately every two years. [1] The period is now often quoted as 18 months by Intel executive David House. This study will examine the development and evolution of semiconductor electronics. Since semiconductors increasingly comprise a larger portion of electronic components and systems, either used directly by customers or incorporated into end use items purchased by consumers, the impact of "Moore's law" has led users and consumers to come to expect a continuous stream of faster, better and cheaper high-technology products. This paper attempts to describe the origin, nature and implications of "Moore's law" in a comprehensive manner. Intel's 32nm, 22nm, 14nm and 10nm technology is examined and studied in detail. Also a retrospective approach to dealing with or coping up with Moore's law is explained. Finally we draw limelight on how Moore's observation transformed computing from a rare and expensive venture into a pervasive and affordable necessity. From internet, to social media and modern data analytics, which are innovations to stem directly from Moore and his findings.

Keywords: Moore's law, semiconductor technologies, faster, better and cheaper high-technology products, Intel's 32nm, 22nm, 14nm and 10nm technology.

I. INTRODUCTION

The invention of the transfer resistor or transistor in 1947 by Bell Laboratory researchers [2] heralded in a new era of solid-state electronics. The concept was based on the fact that it is impossible to selectively control the flow of electricity through a material such as silicon, a solid state material- thus "solid state"- with unique conductive properties, designating some areas as conductor of currents and adjacent areas as insulators, thus the term "semiconductor". Compared with the vacuum tube which was the dominant technology for this task at the time, the transistor proved to be significantly reliable, required much less power, and most importantly, could be miniaturised to almost infinitesimal levels. The 1950's saw a significant progress in solid state research along with the creation of an entire new industry that would design and manufacture semiconductor devices. Although AT&T's Bell Labs is credited with the birth and early development of this new industry [3], a 1956 consent decree ending an anti-trust case prohibited AT&T from marketing commercial solid-state devices and required them to disseminate their patents and technology throughout the industry. Ironically, that very same year three AT&T scientists won the Nobel Prize for their discovery of transistor. [4] Indeed, AT&T's Western Electric would initially become the largest producer of semiconductor to satisfy the device requirements of telecommunications systems. The development of integrated circuit in 1958 represents a major product milestone. Jack Kilby was the inventor of the integrated circuit. [5] A second major breakthrough of the 1950's is better described as a series of incremental process innovations in the manufacturing of semiconductor devices. The two most noteworthy innovations are the diffusion and oxide masking process, and the planar process, both becoming the permanent basis of production since. The diffusion process allowed the producer to diffuse the impurities or dopants directly into the semiconductor surface, eliminating the tedious process of adding conducting and insulating material layers on top of the substrate. The addition of sophisticated photographic techniques permitted the layering of intricate mask patterns in the semiconductor so that diffusion took place only in designated areas. This increased the accuracy of production and reliability of the devices. This planar process enabled the circuits on a single substrate since electrical connections between circuits could be accomplished internal to the chip.

Fairchild introduced the first planar transistor in 1959 and the first planar IC in 1961. Thus the 1959 innovation, planarization is considered as origin of "Moore's law", as the innovation kept the curve of graph as predicted by Moore grow exponentially. Amazingly, the industry has not veered away from the course since then. "Photolithography" enabled manufacturers to continue to reduce the feature sizes of the devices. [6] Thus there was a shift or move from laboratory to production floor and a transition from science to technology.

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In 1965, Moore had been asked to by Electronics magazine to predict what was going to happen in the semiconductor components industry over the next 10 years. He speculated that by 1975 it was possible to squeeze as many as 65,000 components on a single silicon chip occupying an area of only one-fourth of a square inch. [7] His reasoning was a log-exponential relationship between device complexity and time. A new device to be introduced in 1875, a 16k charge-coupled-device (CCD) memory, indeed contained almost 65,000 components. In his paper of 1975 at the IEEE International Electron Devices Meeting, he cited three reasons for the above exponential behaviour:

i. Increase in die sizes at exponential rates.
ii. Simultaneous evolution of finer minimum dimensions (i.e, feature sizes or line widths)
iii. "Circuit and device cleverness."

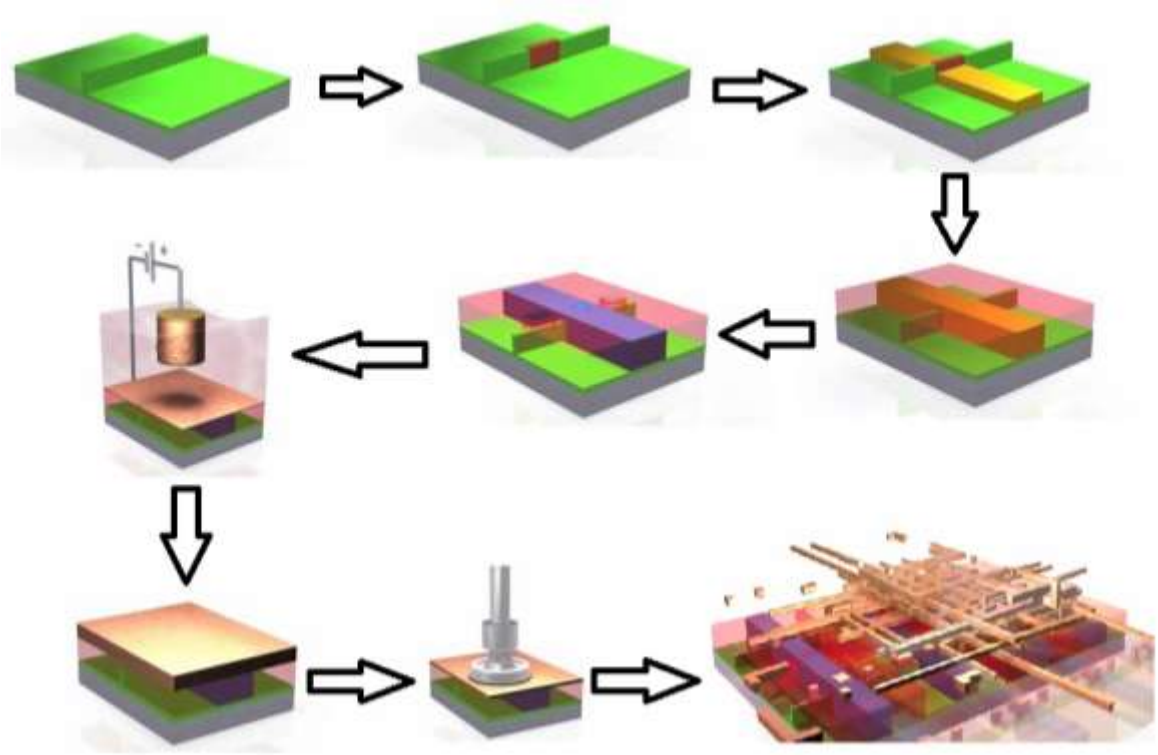

Figure 1 22nm process technology with 3D transistors

Officially, Moore's law states that circuit density or capacity of semiconductors doubles every 18 months or quadruples every three years. The mathematical form of Moore's law is as given below:

(Circuit per chip) = $2^{(\text{year}-1975)/1.5}$

The number of components fitted into a standard size of 16 represents its integration scale, that is, density of components. It is classified as follows [8]:

- SSI- Small Scale Integration
- MSI- Medium Scale Integration
- LSI- Large Scale Integration
- VLSI- Very Large Scale Integration
- VVLSI- Very Very Large Scale Integration
- ULSI- Ultra Large Scale Integration
- GIS- Giant Scale Integration

II. "XX" NANOMETER PROCESS TECHNOLOGY

In this section, we will be studying different "XX" nanometer (nm) process technologies where "XX" may be "45", "32", "28", "22", "14" or "10".

A. 32 nm Technology

Intel had been in high volume manufacturing on its 32nm process technology with second generation high-k+ metal gate transistors since 2009. However 32nm was suppressed by commercial 22nm technology in 2012. The 32nm node

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is the step following the 45nm process in CMOS semiconductor device fabrication. Intel's core i3 and i5 processors, released in January 2010, were among the first mass-produced processors to use 32nm technology. The foundation of the 32nm process technology [9] is the second generation high-k + metal gate transistor. The improvements over the first generation high-k+ metal gate transistors are many. The equivalent oxide thickness of the high-k dielectric has been reduced from 1nm on 45nm to 0.9nm on 32nm process, while gate length has been reduced to 30nm. Transistor gate pitch continues to scale 0.7 times every two years. The 32nm uses the same basic metal gate replacement process flow as Intel's 45nm process technology. The decreased oxide thickness and reduced gate length enables a >22% transistor performance gain in terms of drive current.

B. 22nm Technology

22nm technology suppressed the 32nm technology after its release into the market in 2012. Intel had deployed a family of 3D transistors manufactured at 22nm. These new transistors enable Intel to relentlessly pursue Moore's law. Earlier, the transistors which used for the core of the microprocessors were 2D (planar) devices. The Intel 3D tri-gate transistors and the ability to manufacture it in high volume marked the dramatic change in the fundamental structure of the computer chip. The Intel 3D tri-gate transistor uses three gates wrapped around the silicon channel in a 3D structure, enabling an unprecedented combination of performance and energy efficiency. It was designed to provide unique ultra-low power benefits for use in hand-held device like Smartphones and tablets.

Figure 1 shows the 22nm process technology with 3D transistors. Figure 2 shows a transistor with a stream of electrons flowing over a plane. The gate is made of metal over high k insulator, controlling the flow of the electricity in that stream and acts as an ordinary switch turning flow on and off. The key objective of transistor design is maximum current flow in the ON state and zero current flow in the OFF state.

Figure 3 shows the 3D 22nm process technology transistor. In this 3D transistor, the 2D flat stream is replaced with 3D fins, where the flow will be on all "three" sides of the fin compared to "one" as in the planar transistor and is called "tri-gate" transistor capable of operating at low voltages and with reduced leakage current, thereby increasing performance and energy efficiency.

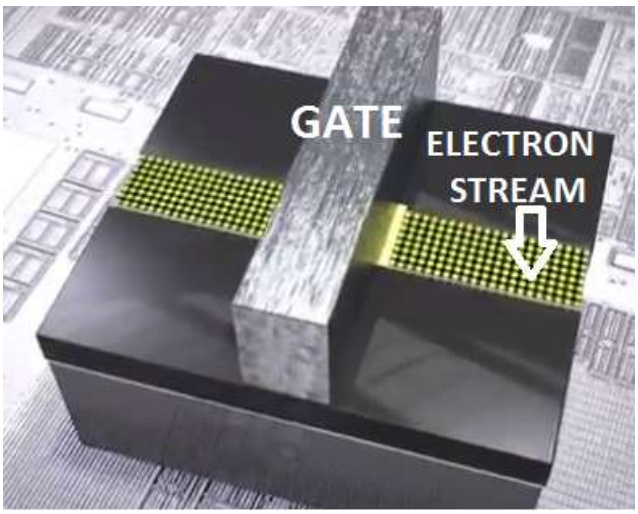

Figure 2 Transistor with a stream of electrons flowing over a plane

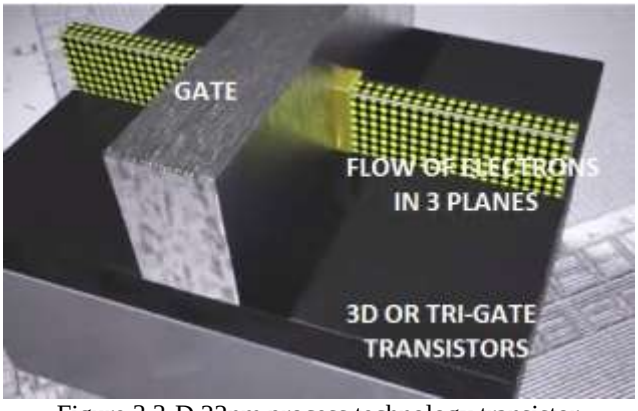

Figure 3 3-D 22nm process technology transistor

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C. 14nm and 10nm Technology

The 14nm semiconductor fabrication node is the technology following the 22nm node. Supporting a wide range of devices from mobiles to servers, 14nm transistors improve performance and reduce leakage power. Intel 14nm technology uses 2nd generation 3D tri-gate transistors. Intel 14nm technology provides good dimensional scaling from 22nm. The transistor fins are taller, thinner and more closely spaced for improved density and lower capacitance.

Figure 4 shows the 14nm process technology. In the previous section, only one tri-gate fin was shown, but now multiple tri-gate fins which are taller, thinner and closely spaced. This improved technology provides three major benefits:

- Faster, allowing more processing
- Requires less active power- leading to longer battery life.
- Eco-friendly – less carbon foot print.
- Less area required per transistor

10nm process technology is the proposed successor of the 14nm node technology. The extensive use of ultra-low-k dielectrics means that conventional photolithography, etch or even chemical mechanical polishing processes are unlikely to be used, because these materials contain a high density of voids and gaps. At the ~10nm scale, quantum tunnelling becomes a significant phenomenon.

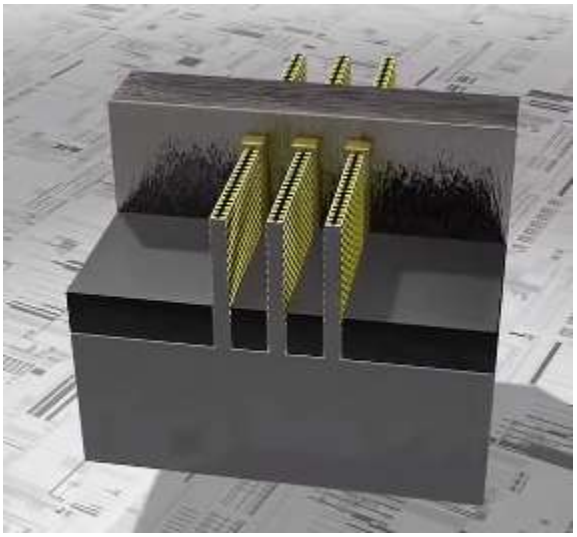

Figure 4 14nm process technology

III.TIME SCALING IN THE 4TH DIMENSION

Moore's law of exponential growth predicted doubling of processor speed per unit area on silicon microchips with a doubling period of 18 months. This has continued to be the case ever since Gordon Moore first postulated this notion in a publication in 1965. Some researchers have estimated that Moore's law will reach its physical limits in the next 15-20 years. Notably, the rate of growth has notably begun to decay over the past decade and viable alternatives that provide equal or superior processing speeds for computations are already in research and development stages.

The idea is to increase the speed of processing without increasing the density on the chip, because the scaling down process has reached saturation and no more scaling down is possible. How about exploring the 4th dimension – "The Time" when no more scaling down can happen in the other 3-Dimesions – i.e. length, width and height? The idea is to have a retrospective processing approach rather than instantaneous real time processing.

Take three instances t_1, t_2 and t_3. t_1 is the first instance followed by t_2 and t_3 which are second and third instances respectively. Suppose 20 units of processing has to happen in the 1st instance, this can be shared with the other two instances t_2 and t_3 which are future instances and are most likely to happen. So the processing will be done in future, by predicting the earlier instances and by the time it is t_2 or t_3 instance, the process would have already been taken place thereby reducing the burden on the present. For example 20 units can be intelligently shared between t_1, t_2 and t_3. It is nothing but processing the desired number of units in the future at the same time as processing taking place in the present. It is similar to time travelling. This increases the processing speed and also low power is dissipated or uniform power is dissipated. So when the three dimensions are saturated, the fourth dimension can be exploited to keep up with the Moore's prediction in terms of processing power or chip. Also note that the intervals between t_1, t_2 or t_2, t_3 is in nanoseconds or even less.

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IV. CONCLUSION

Though the Moore's law has ruled the semiconductor industry for over a period of 50 years, each new process node is getting tougher and tougher to make because it incorporates new manufacturing tools, processes, materials and approaching the limits of atomic structures. One may ask the question "Is the Moore's law here to stay?"; "If yes, then how long?" as the great man Gordon Moore himself acclaims, "Frankly, I didn't expect it to be so precise."

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BIOGRAPHIES

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